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Energy Efficient Decoding Using Analog VLSI Techniques

Low-density parity-check (LDPC) codes have become one of the preferred methods for forward error control in digital communications systems. These codes approach the Shannon capacity limit, and as such address the issue of transmit power. However, the use of such coding techniques also incurs a computational energy cost at the receiver that is not traditionally accounted for in the code design process. LDPC decoding is typically conducted using a message-passing algorithm that runs over a graphical representation of the code. Typical graphs may have tens of thousands of connections, each requiring several multi-bit messages to be passed during a decoding cycle, and perhaps requiring aggregate signaling rates on the order of Terabits per second! Since dynamic power consumption in a VLSI chip is related to the signaling rate, this represents a considerable challenge. In this talk I will present message-passing VLSI architectures that are guided by these computational energy constraints.

Analog decoders are message passing decoders that process LLR messages in continuous-time and using continuous-valued voltages and currents to represent likelihood messages. Only the outputs of decoders are binary, and as such analog decoders do not require high-speed analog-to-digital converters as a front end. Such decoders, often based on the Gilbert multiplier using sub-threshold mode CMOS transistors, have been shown in physical measurements to be computationally efficient. This talk will provide an introduction to the circuits used in such analog decoders, as well as the design challenges and limitations of the technology.